

FIG. 1 PRIOR ART

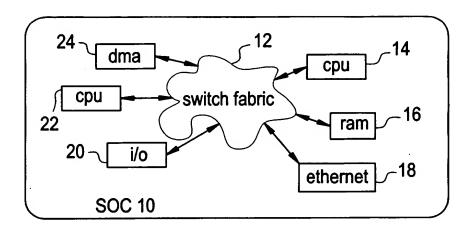


FIG. 2

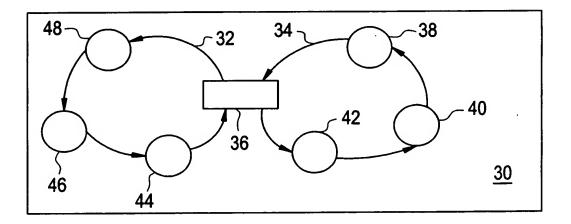






FIG. 3

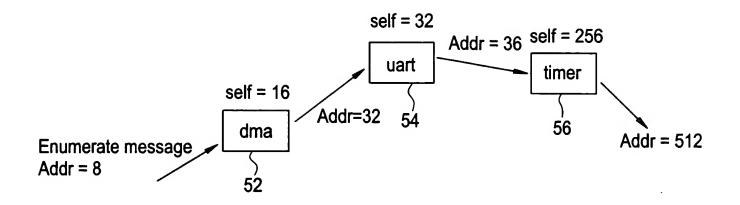


FIG. 4

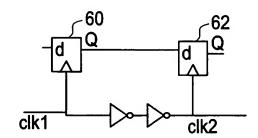


FIG. 5

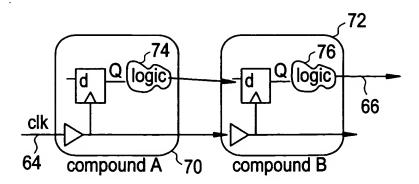






FIG. 6

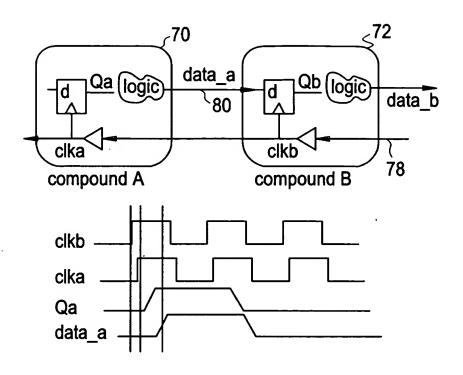


FIG. 7

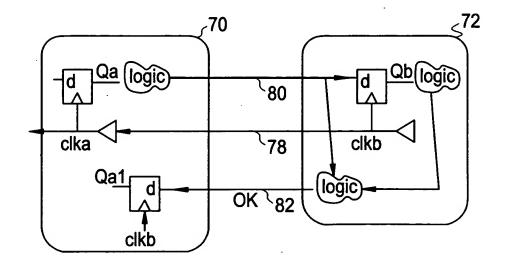




FIG. 8

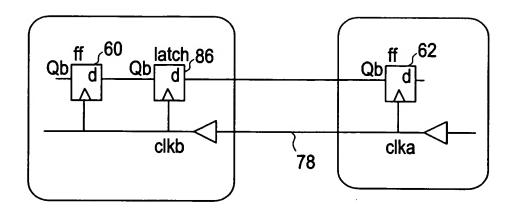
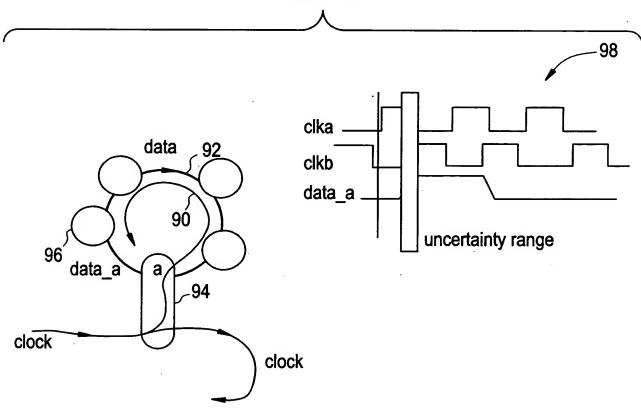
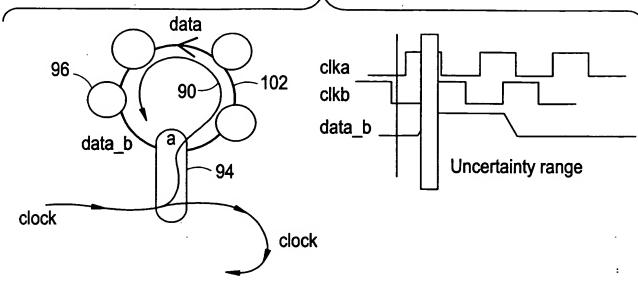


FIG. 9



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FIG. 10



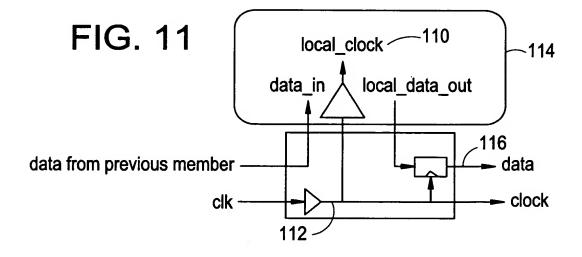


FIG. 12

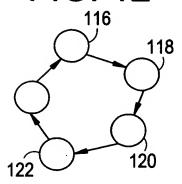
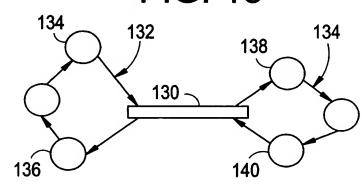


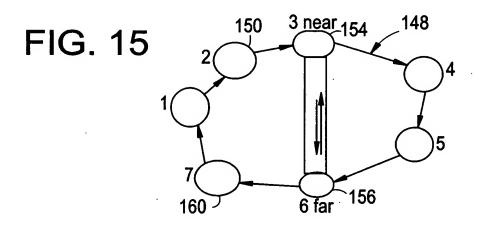
FIG. 13





-154 150 FIG. 14 158 -146 152 160 148

156



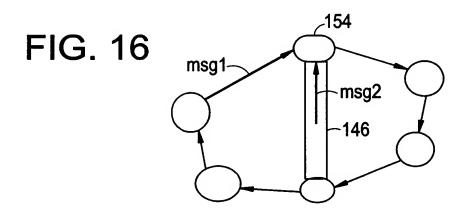




FIG. 17

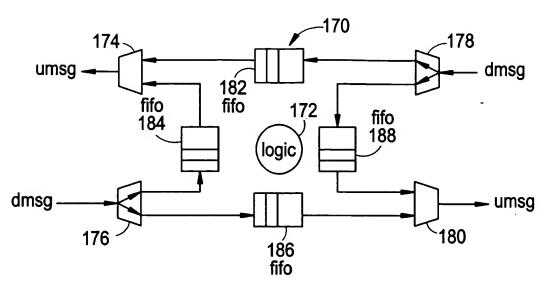
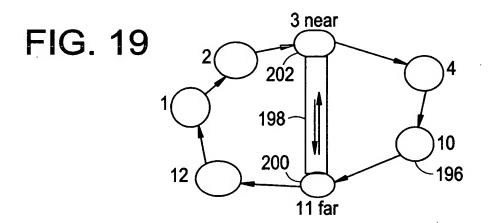
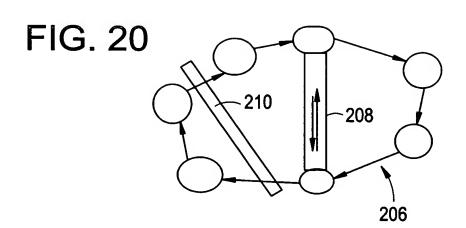


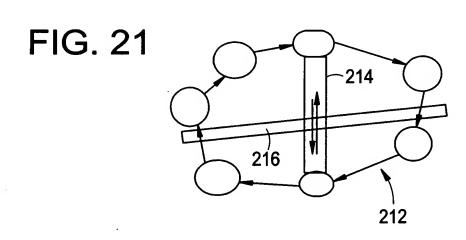
FIG. 18

192

near far







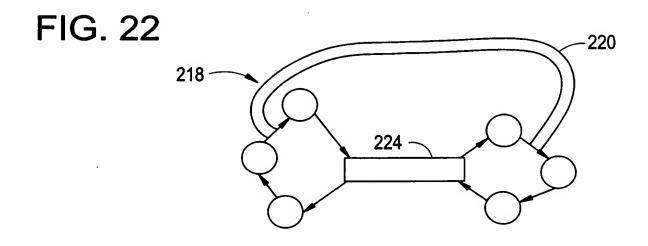


FIG. 23

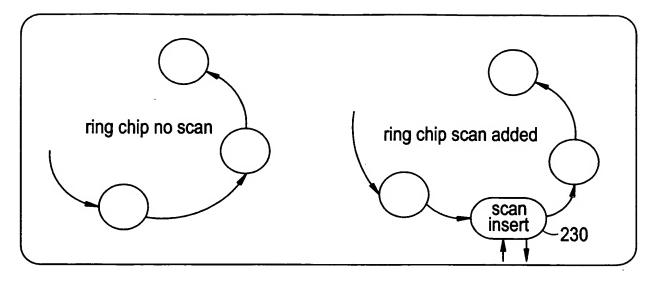


FIG. 24

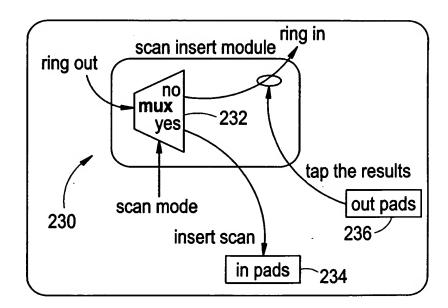


FIG. 25

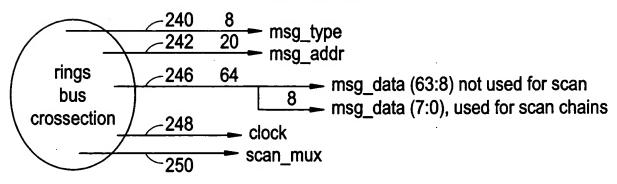




FIG. 26

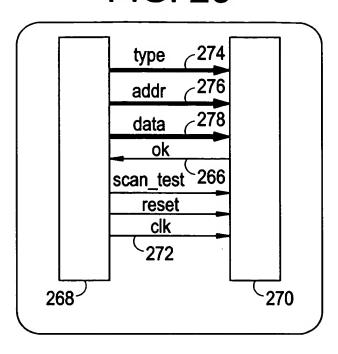


FIG. 27

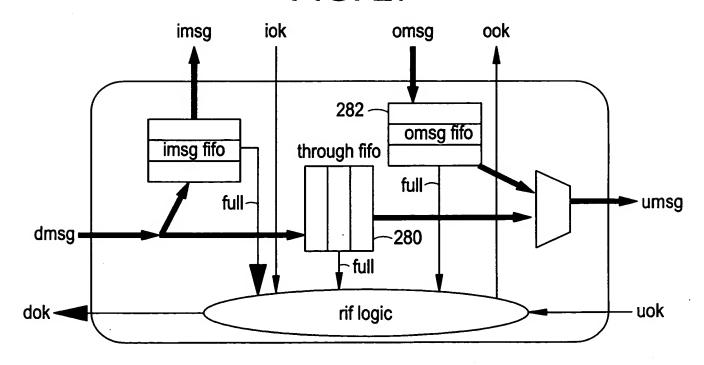




FIG. 29

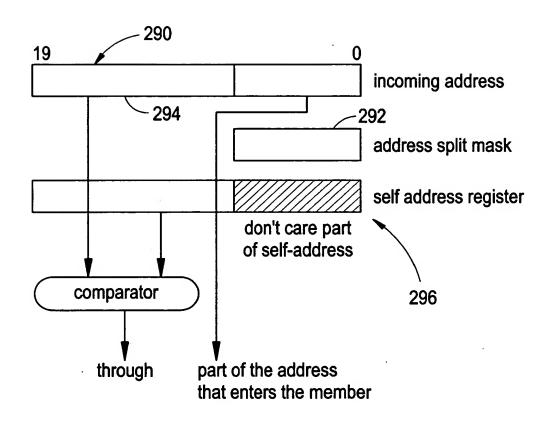




FIG. 30

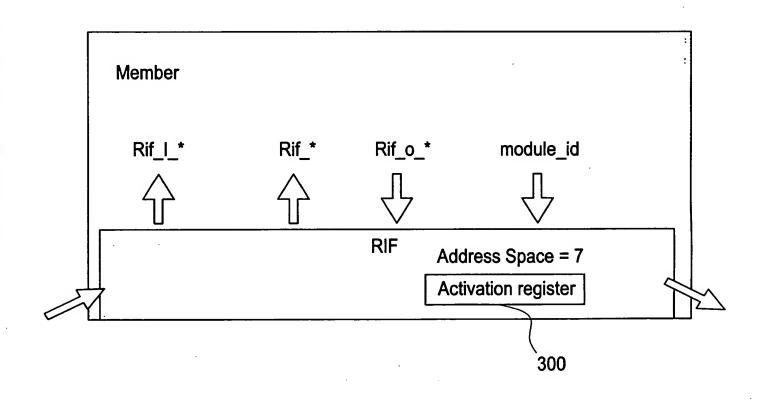




FIG. 31

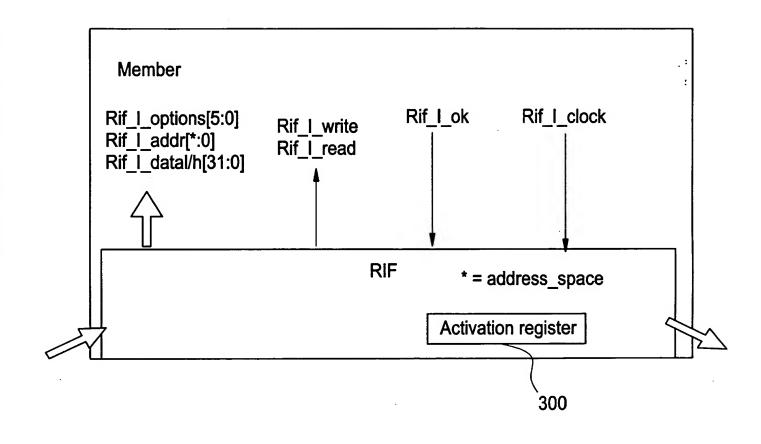




FIG. 32

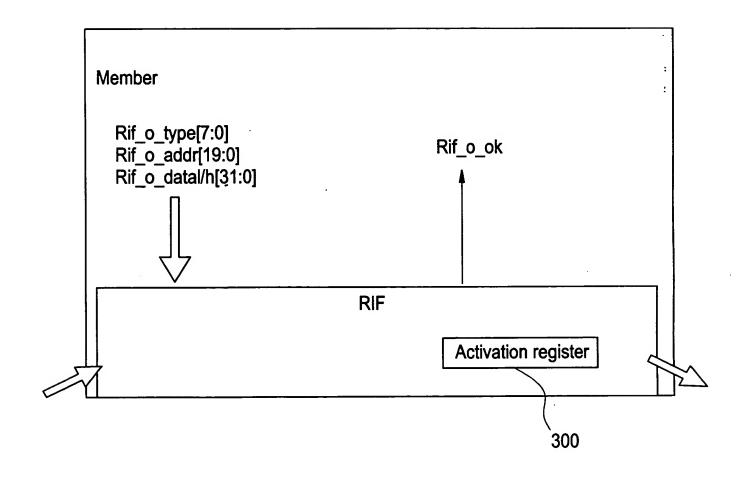
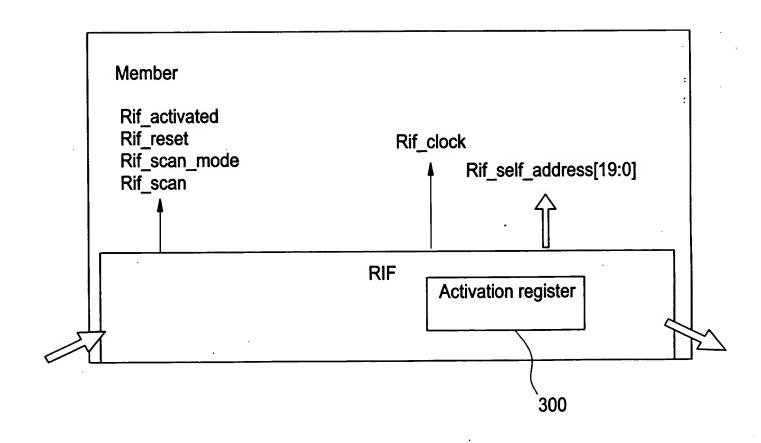




FIG. 33



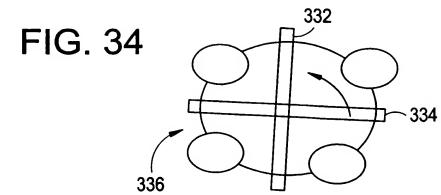
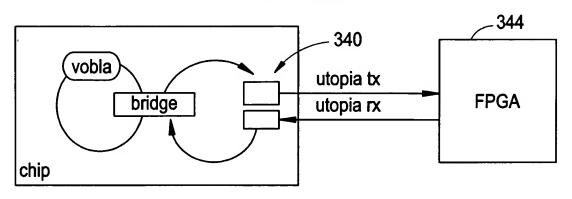
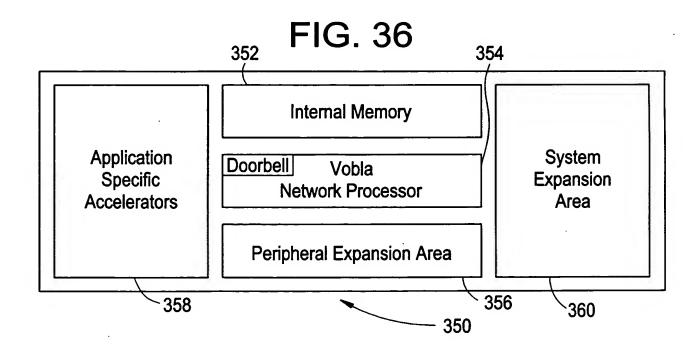


FIG. 35





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(spr index - 3)



21/64

FIG. 41

R1 register

FIG. 42

mb - reflection of the RAM mult-reader busy indication

REFETCH SPR **NEXT REFETCH** REFETCH (spr index - 0) 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0 10987654321 0 9 8 7 6 5 4 3 2 1 0 DOOR UMASK NTID **CTID** TASK SPR COUNT (spr index - 1) 442 19876543210 3 Y T D P T B B A A R B B A TRAP SPR (spr index - 2) 9876543210 0987 INDEX1 MINDEX SPR INDEX2

446



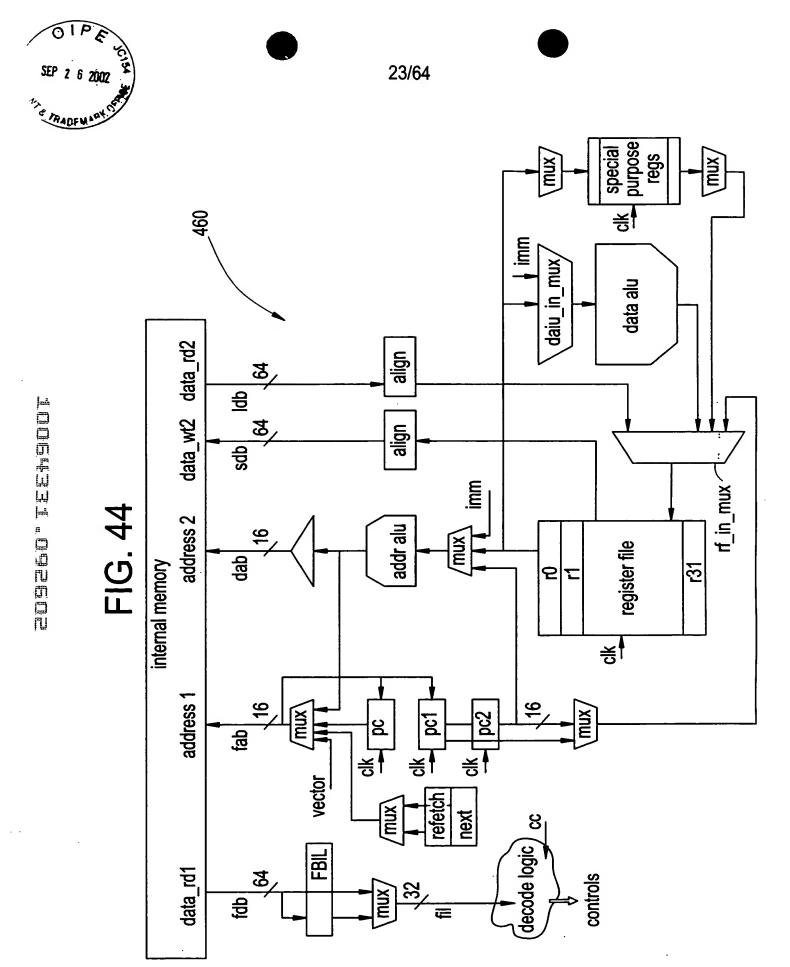
FIG. 43

	450		
	common task data		
	task		task
r27	fragment 1 data	task fragment 2 data	fragment 3 data
	data of all level2 functions		
	level1 f1 data	level1 f2 data	level1 f3 data

size of level0 frame part is different for each task type

size of level2 frame part is constant size of level1 frame part is different per each task

type



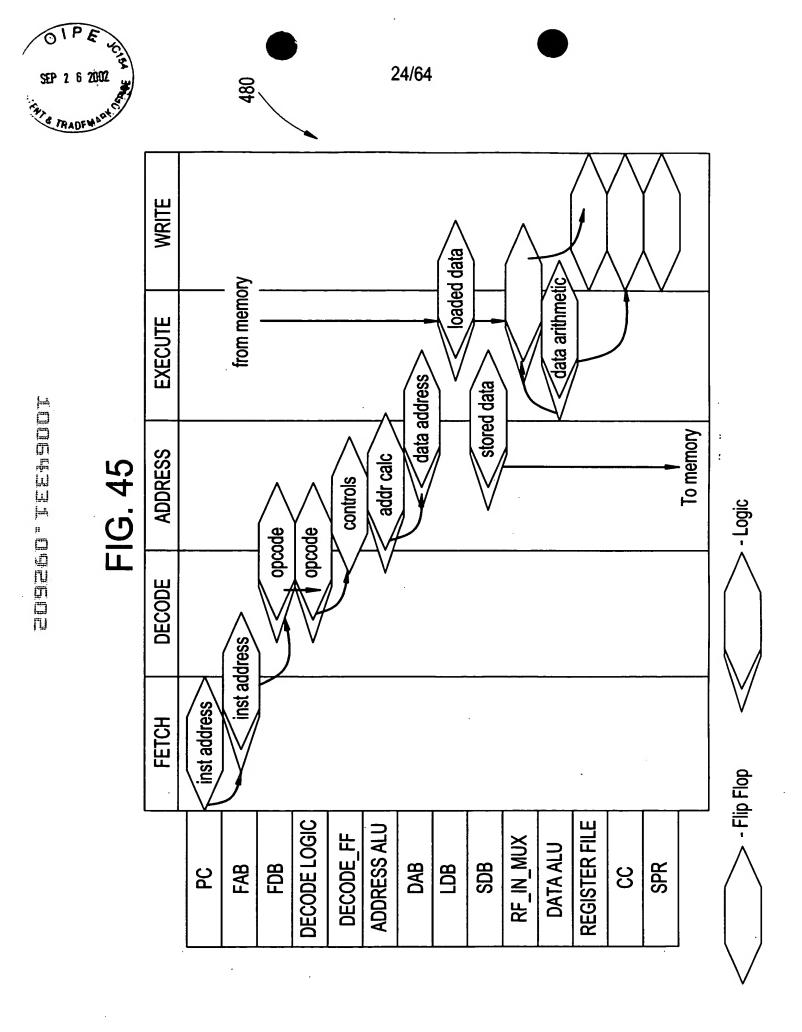




FIG. 46

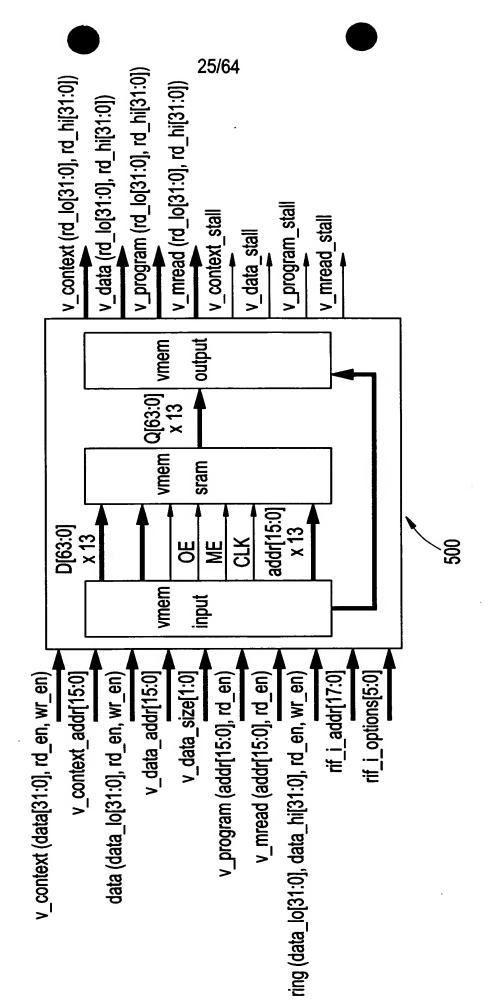
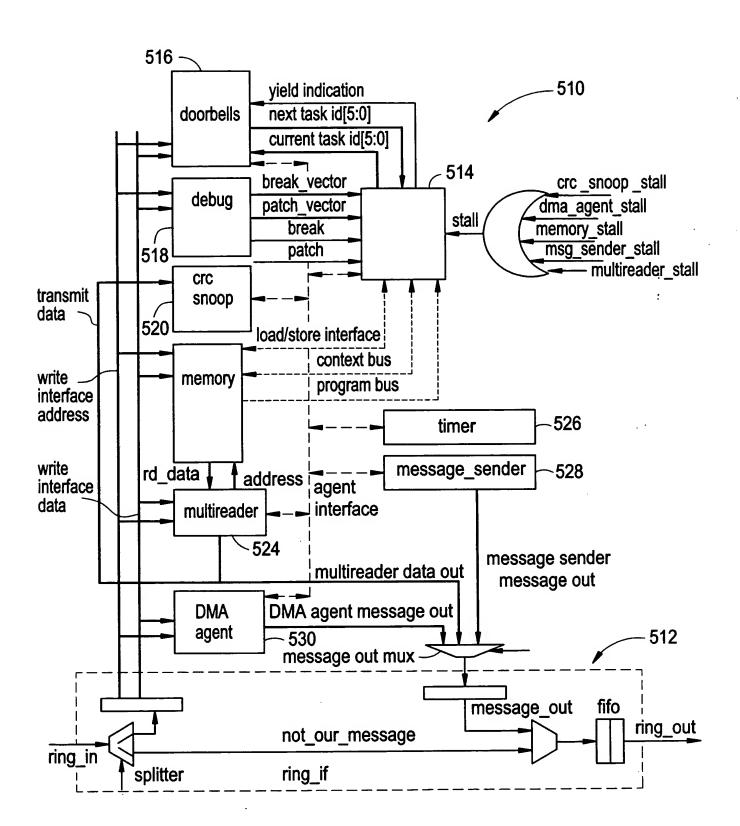
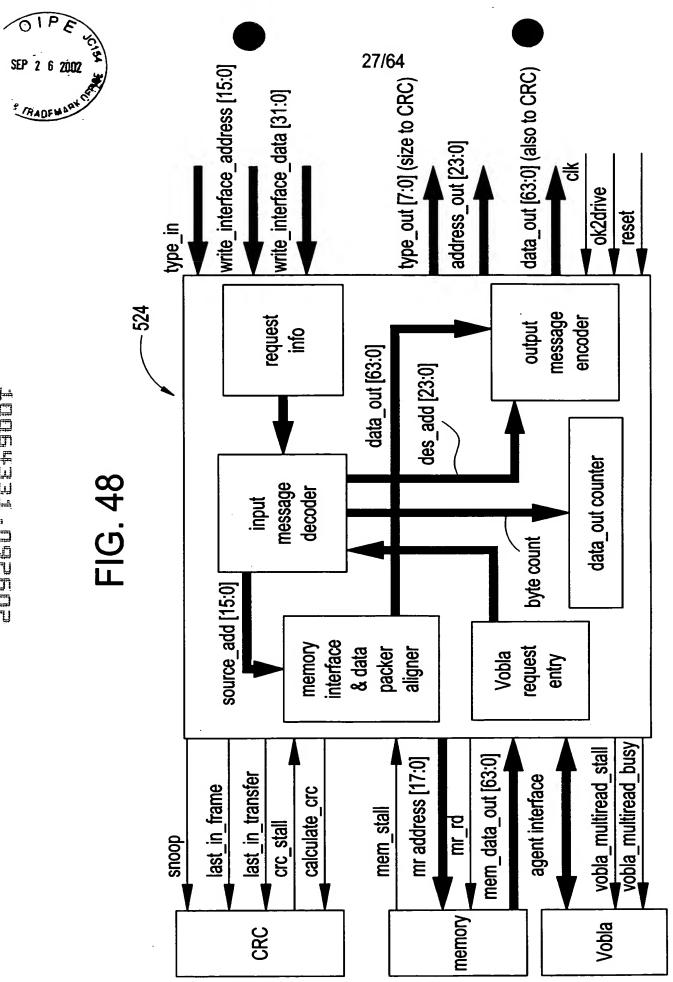




FIG. 47



TOOSHIIL CENDOUT



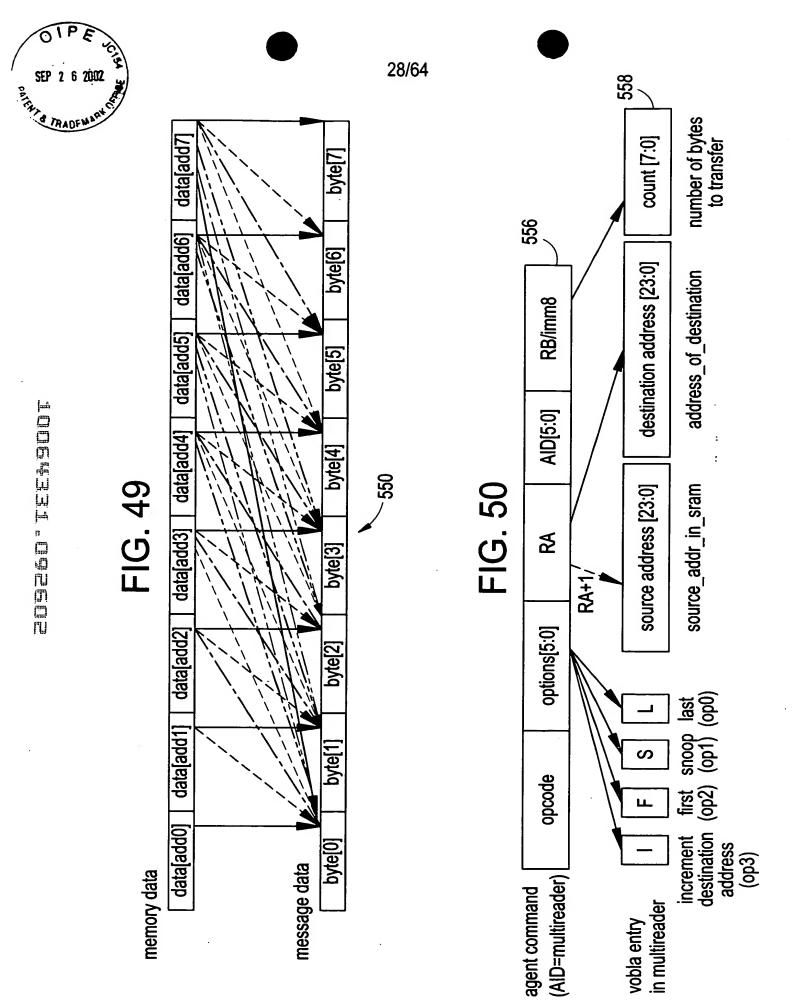
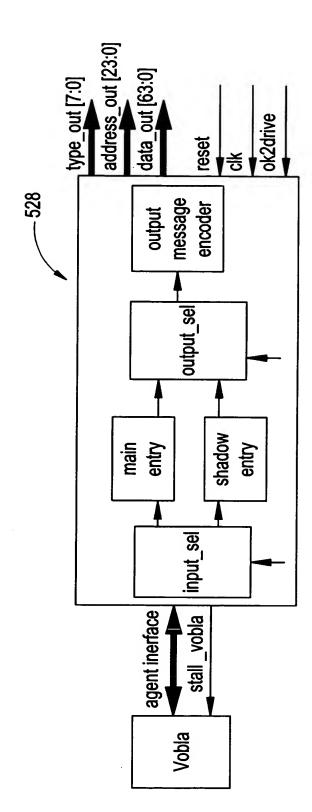




FIG. 51







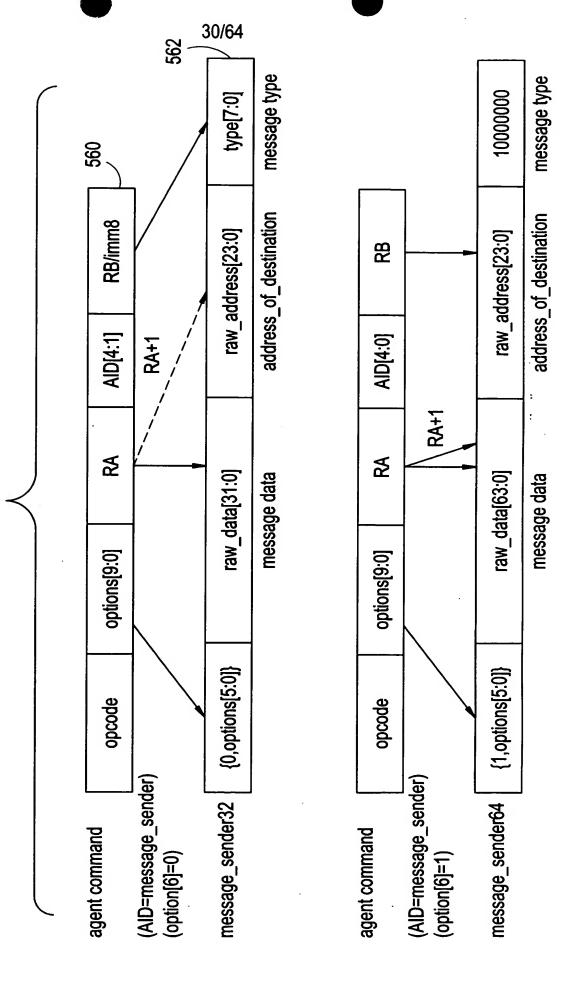




FIG. 53

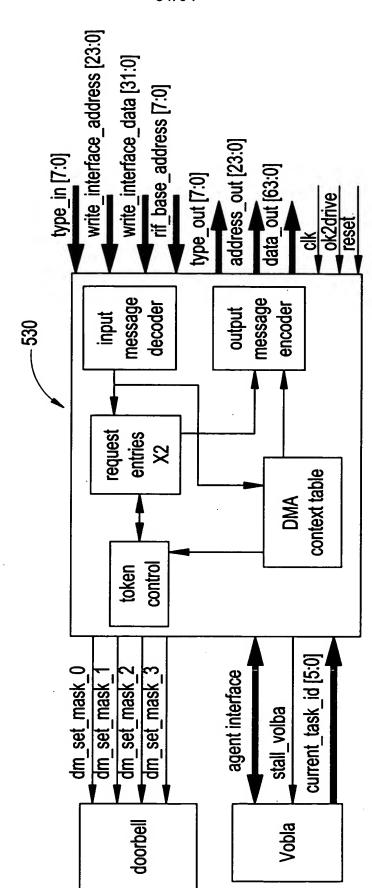




FIG. 54

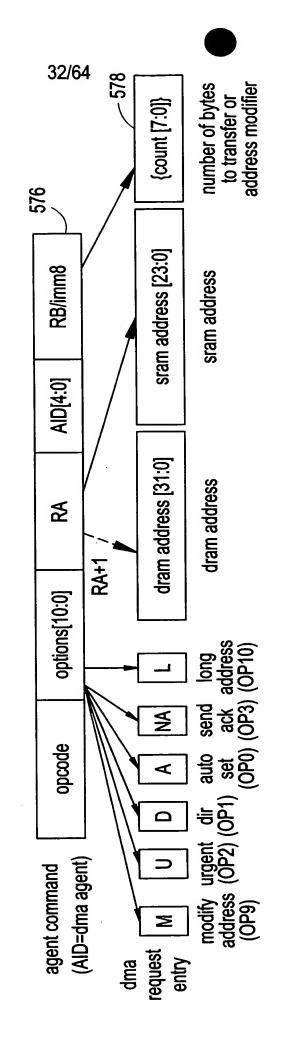




FIG. 55

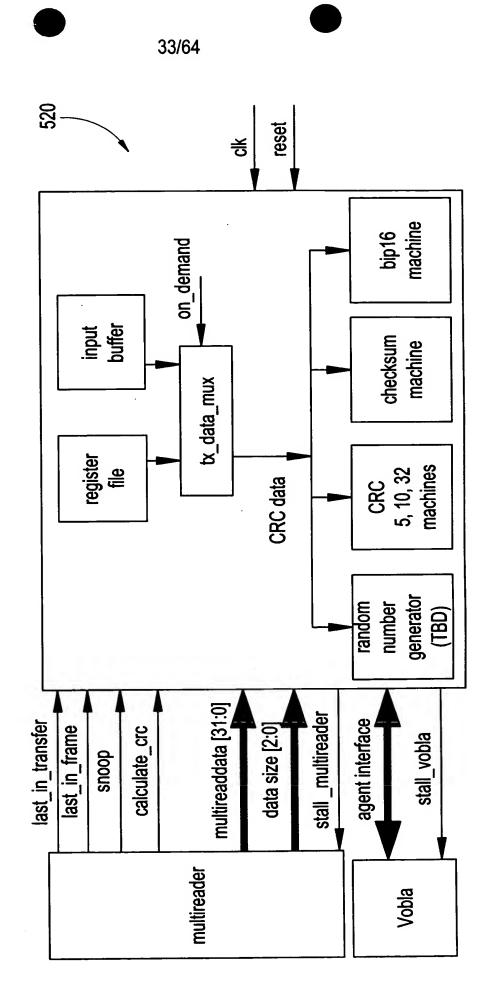




FIG. 56

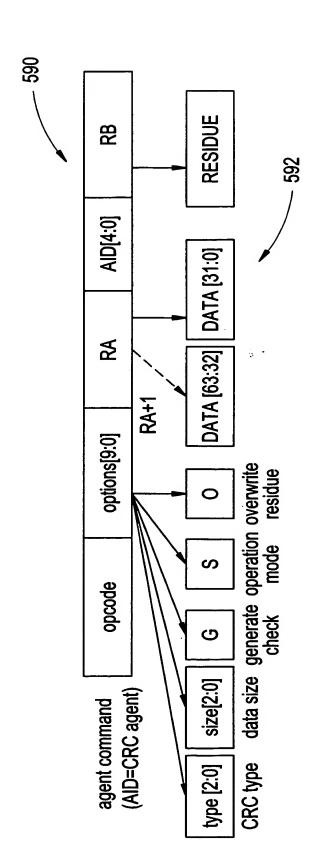




FIG. 57

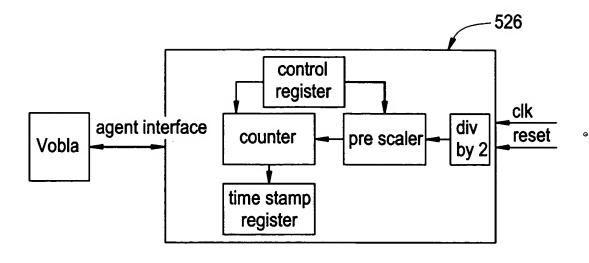
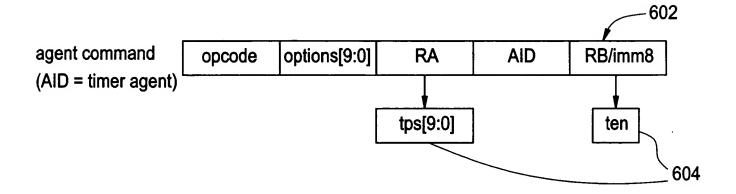


FIG. 58



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{1,1,0,0,0,0,0, urgent_value} write urgent

(0,1,0,0,0,0,0,0) write TGMR

614

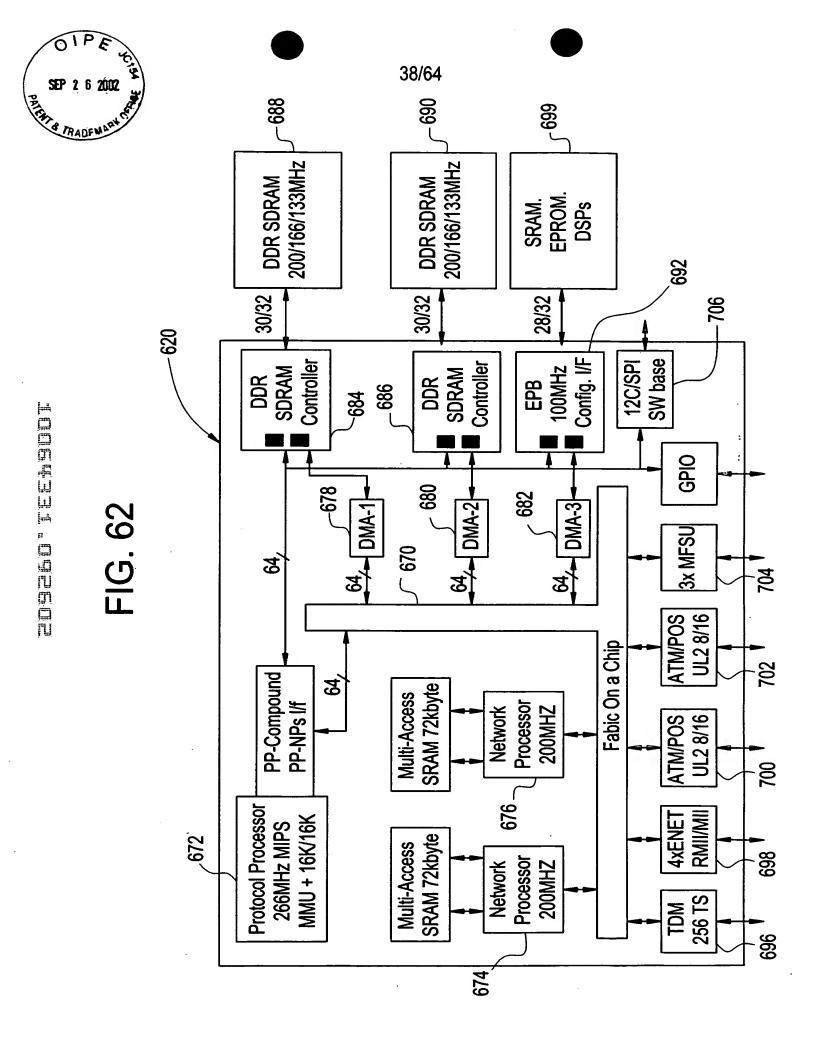




FIG. 63

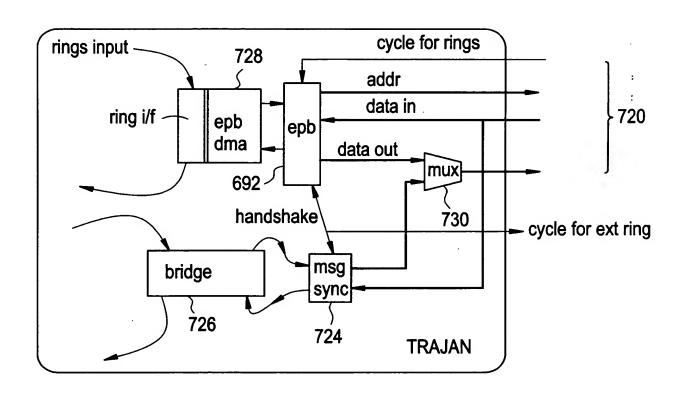
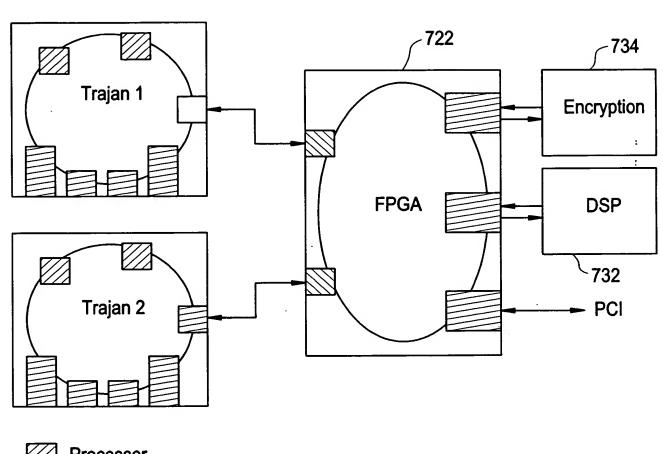




FIG. 64



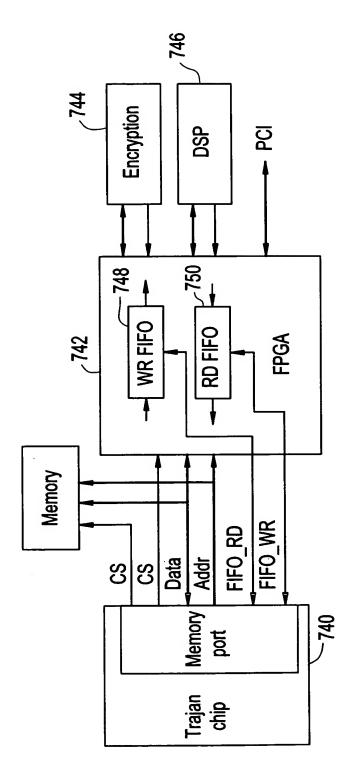
Processor

Functional unit

External ring interface



FIG. 65



:

:



FIFO_WR FIFO_RD ADDR DATA -760 ഗ് Memory controller Trajan 740 Read request FIG. 66 RD FIFO used words counter generator Message sender Host #2 (DMA) Host #1 (PP) . Host #3 (Ring extender) WR FIFO used words counter Write request generator DATA DATA 옷 옷 interface Ring



FIG. 67

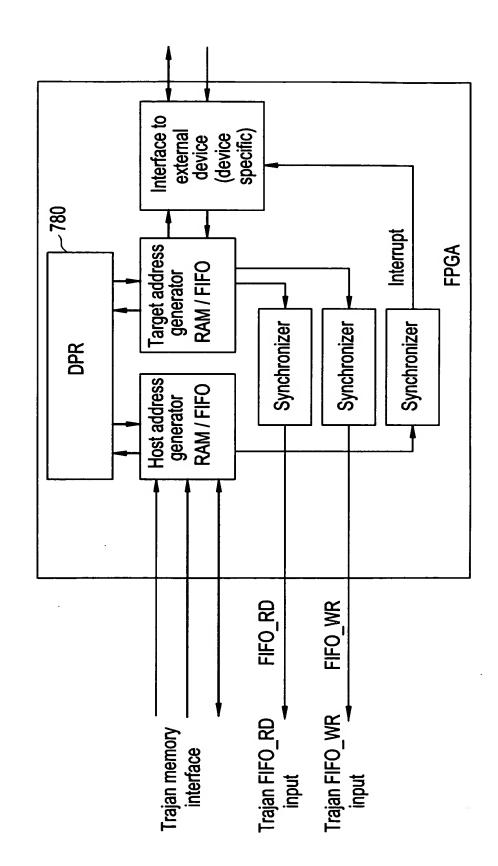




FIG. 68

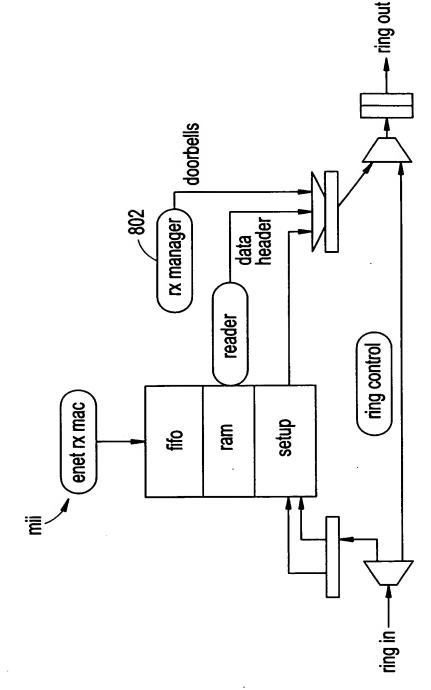




FIG. 69

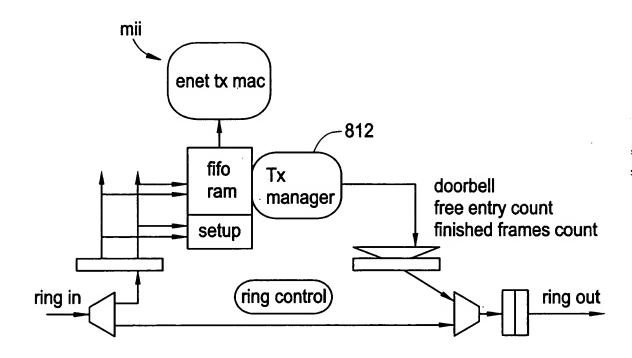
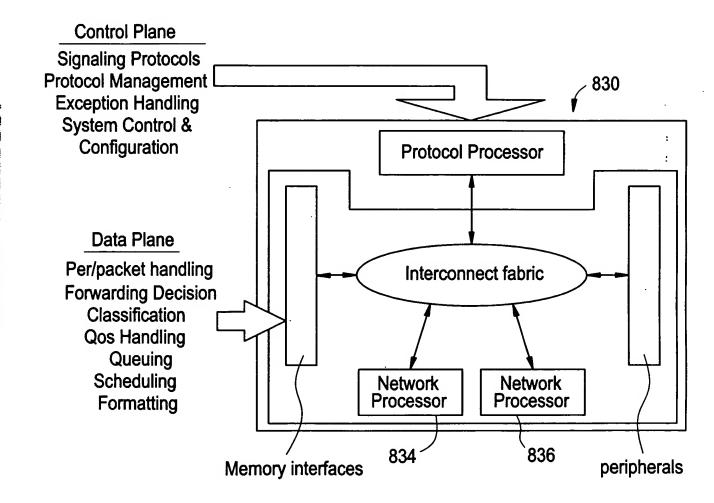
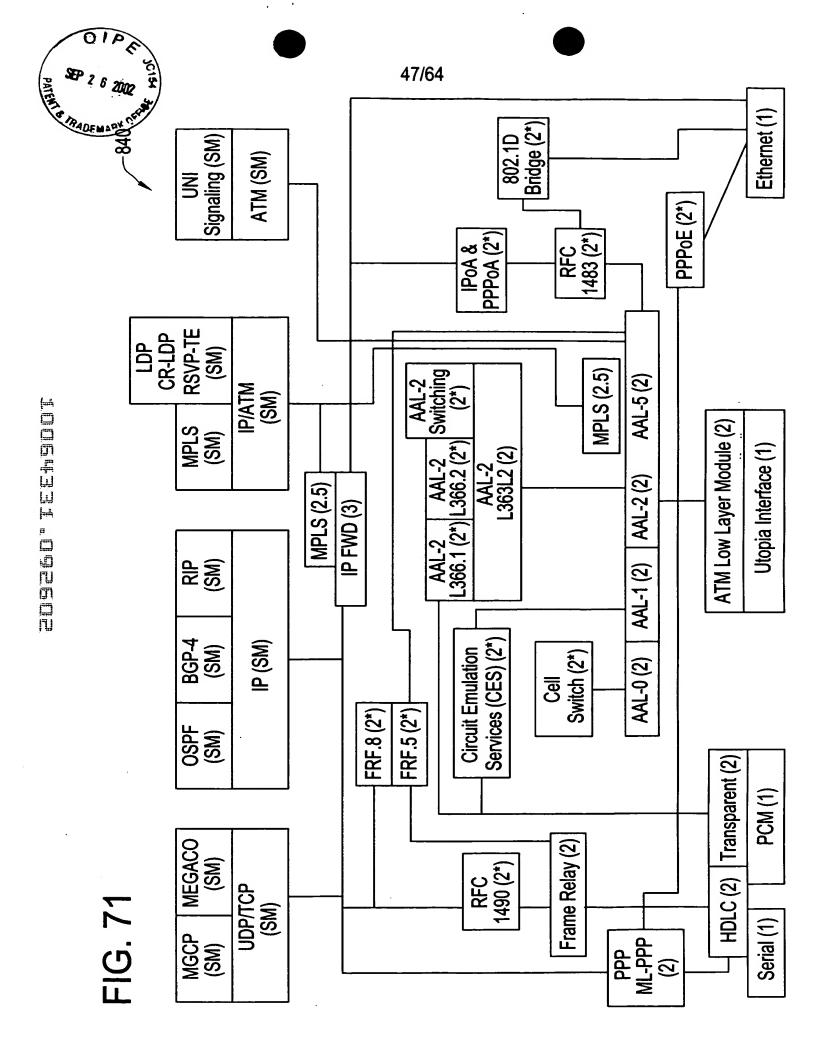




FIG. 70





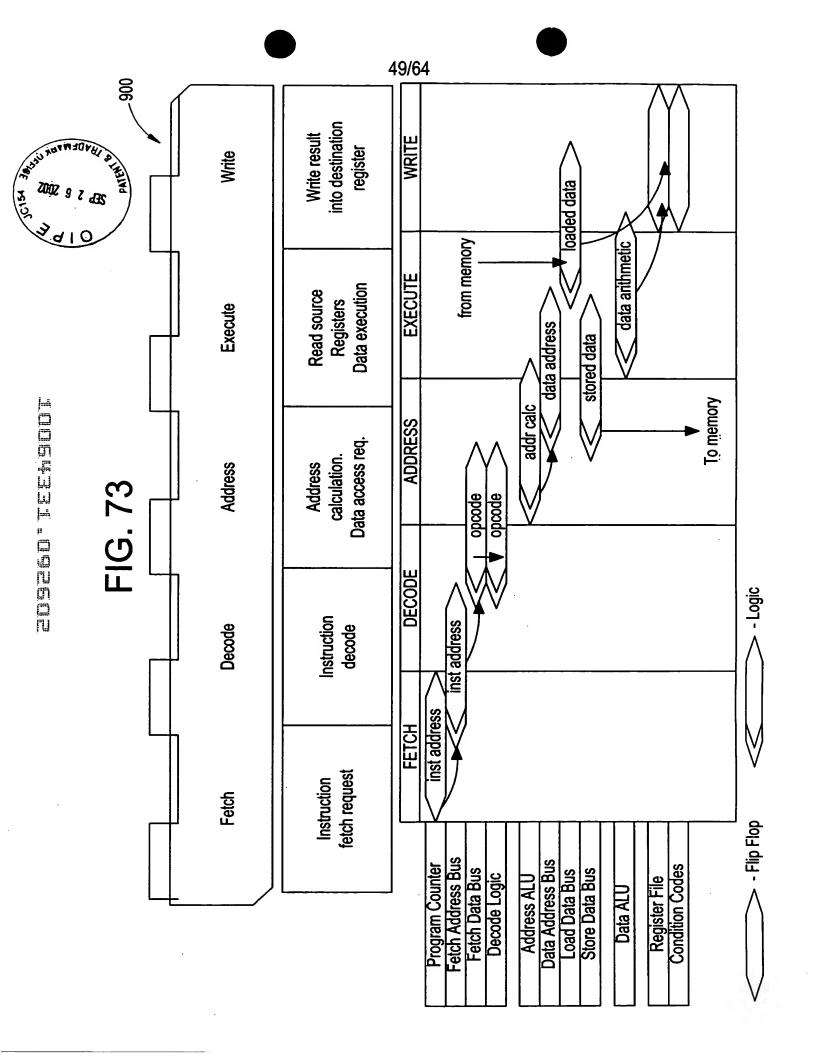




FIG. 74

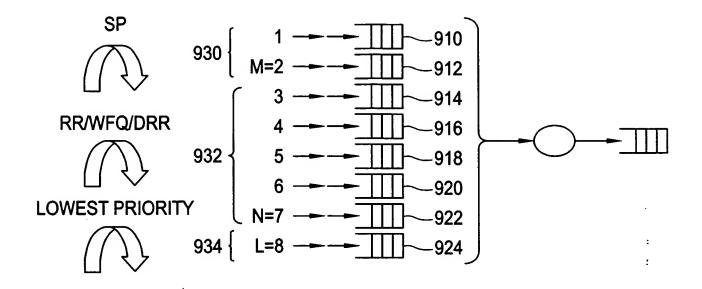
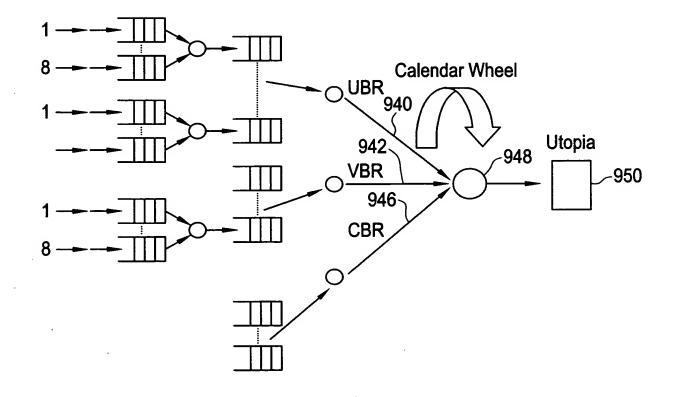
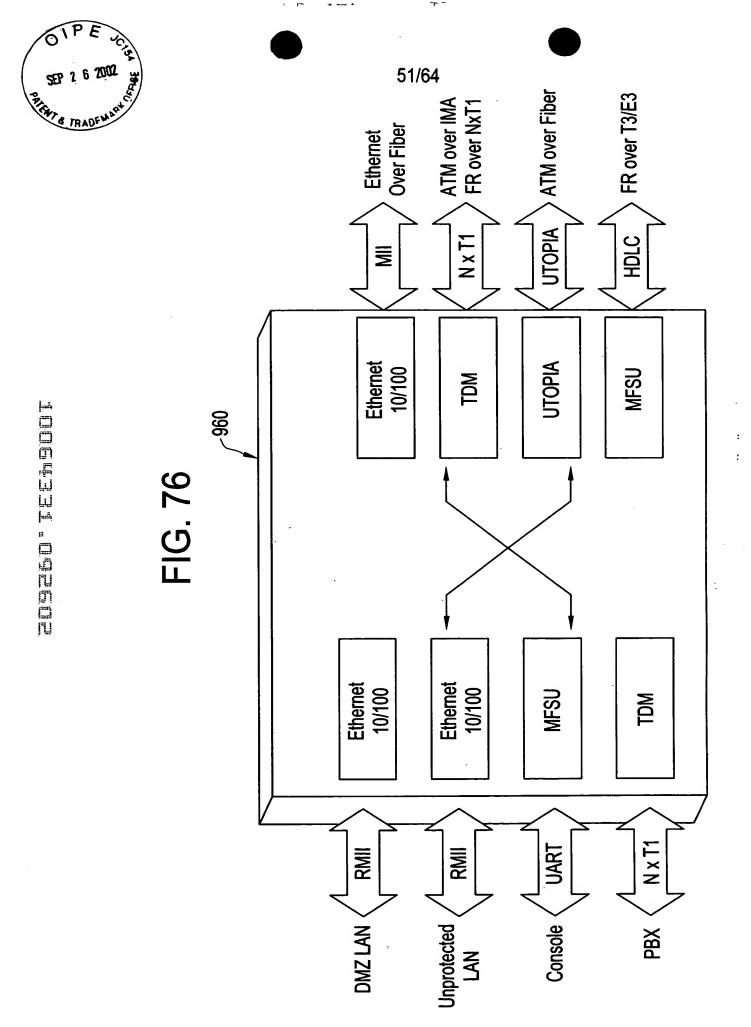
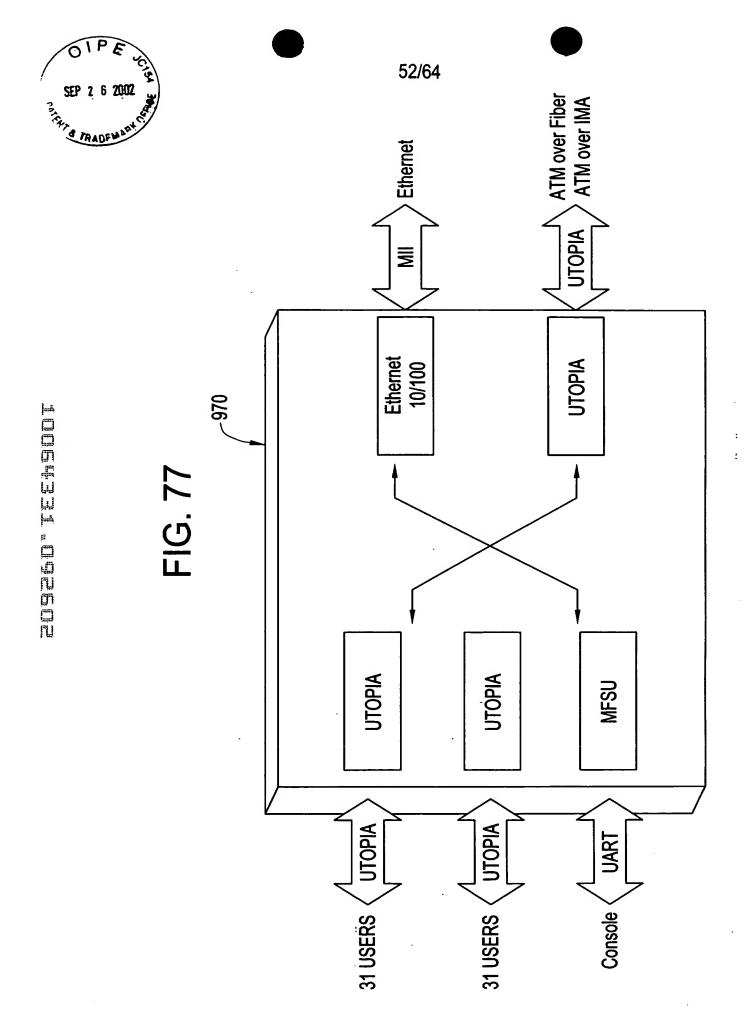
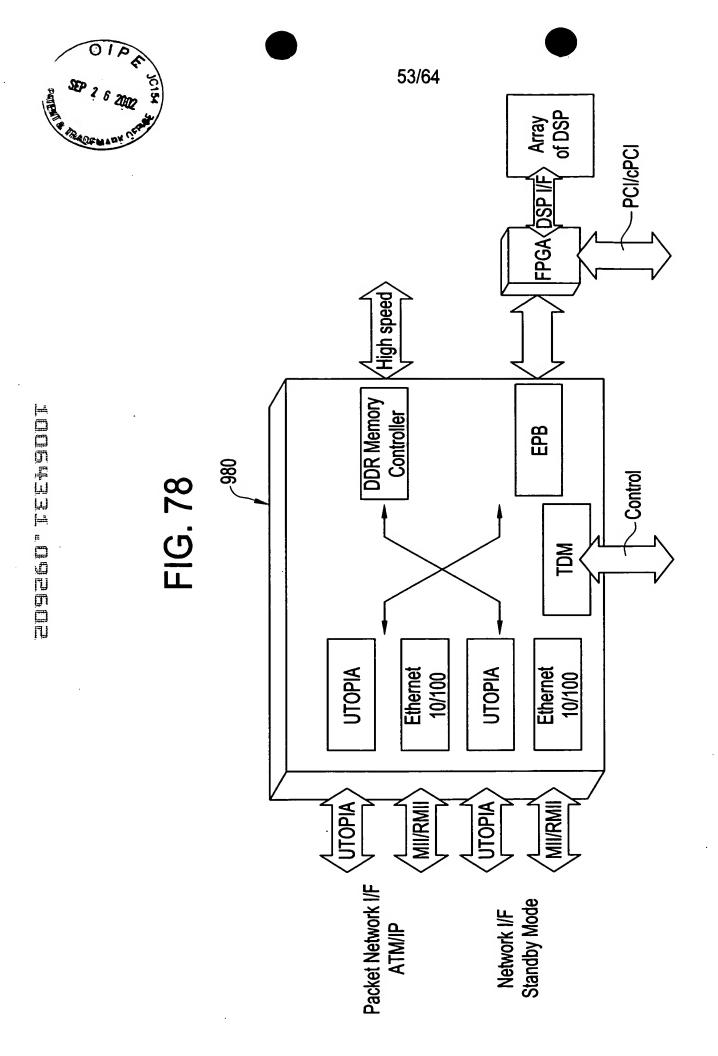


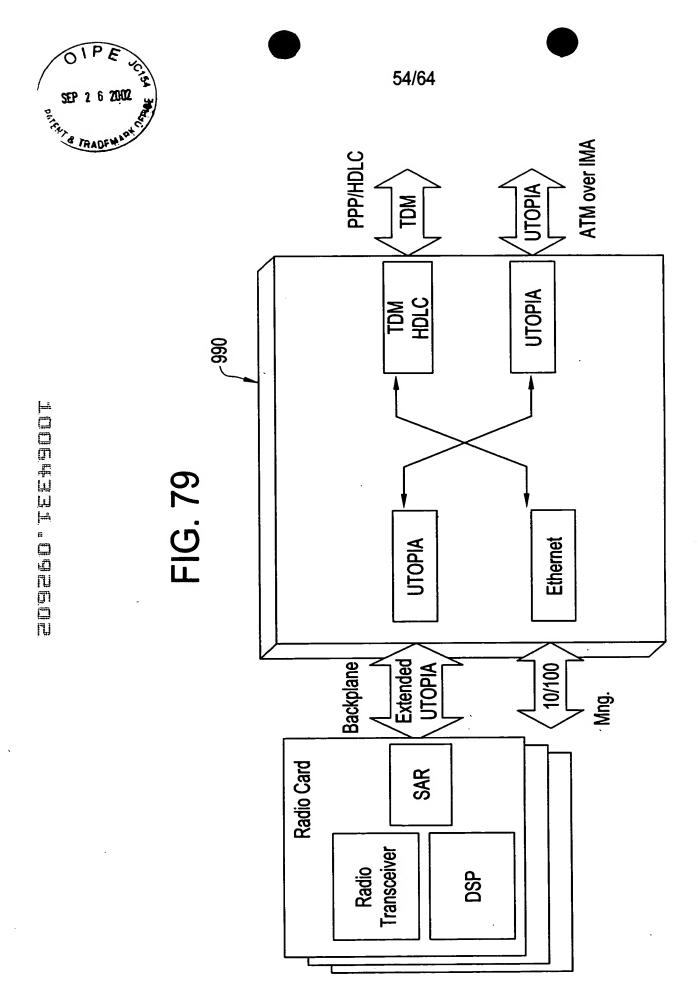
FIG. 75











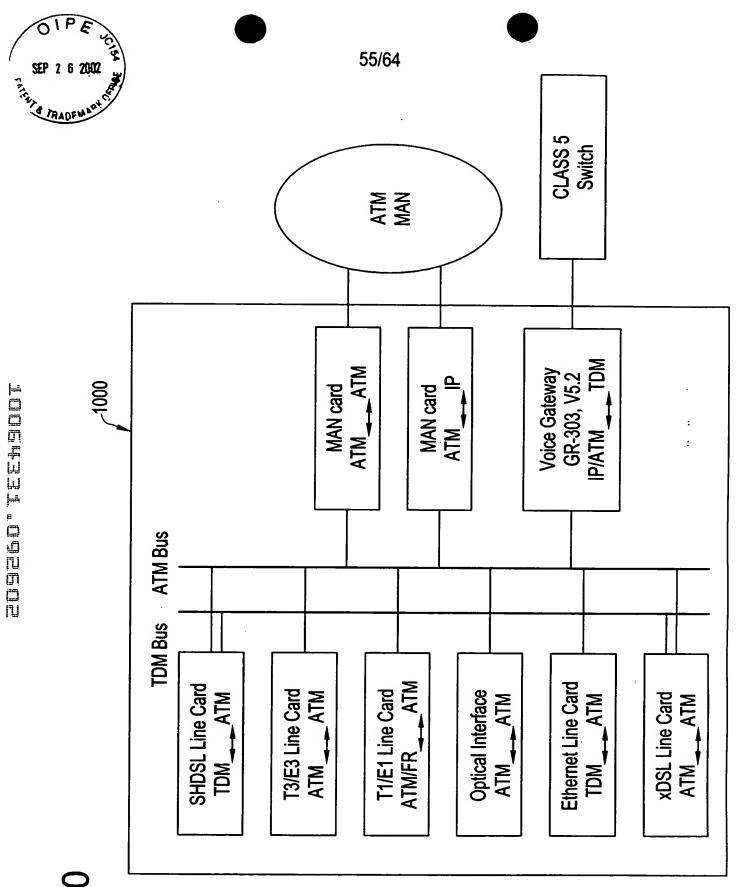
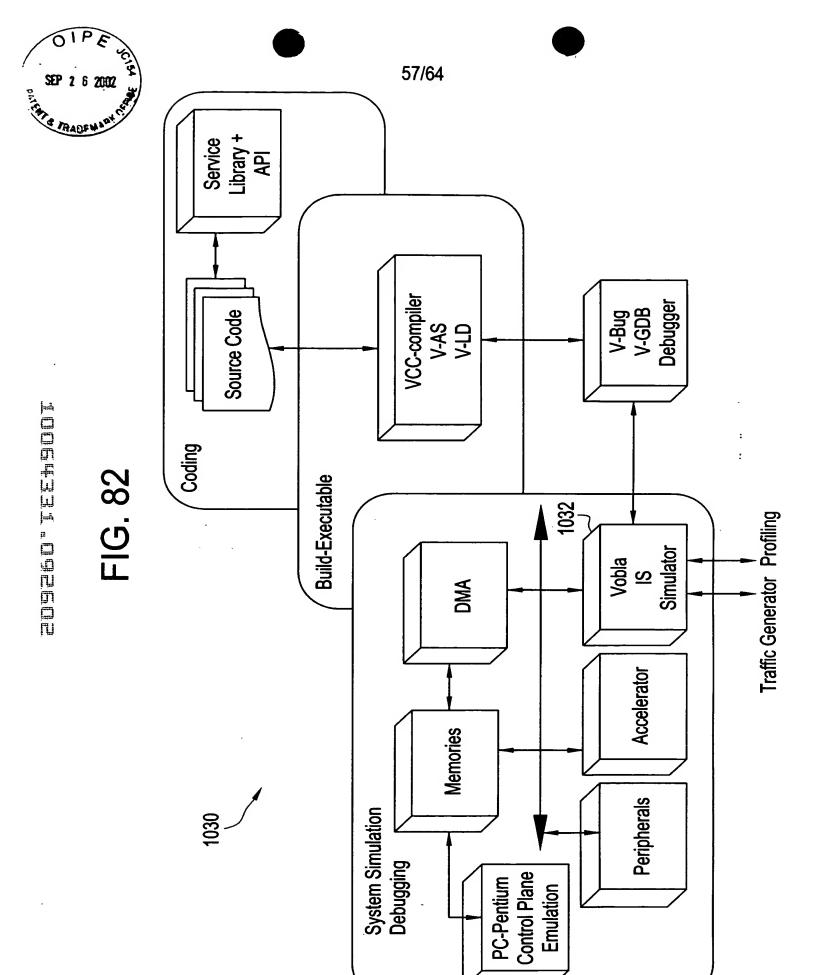
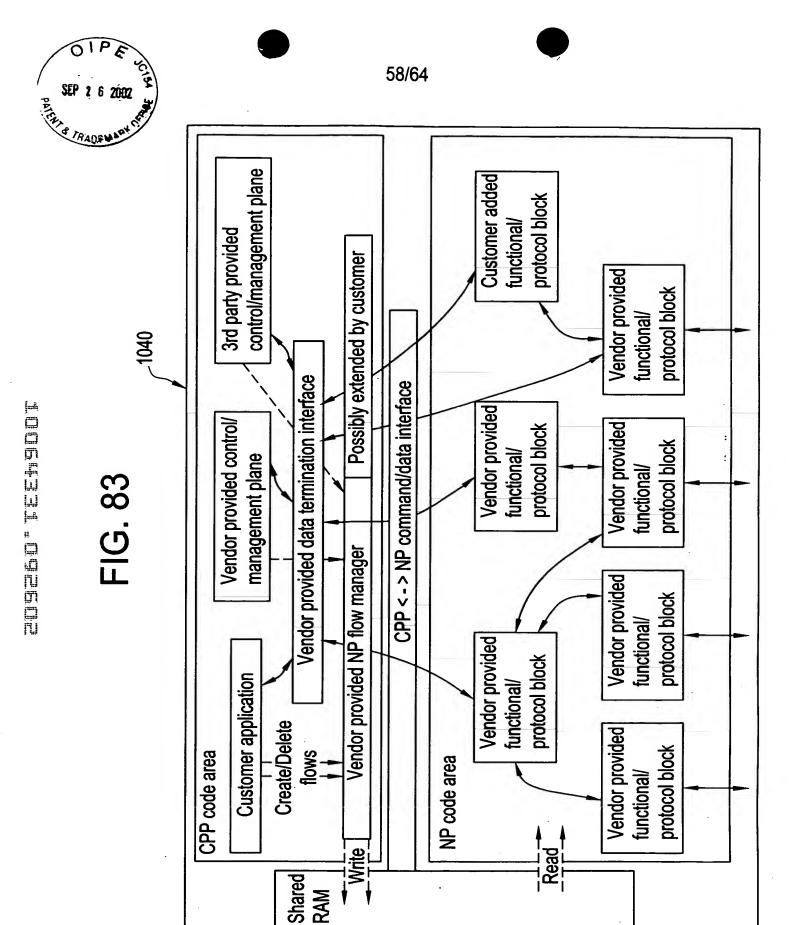


FIG. 80

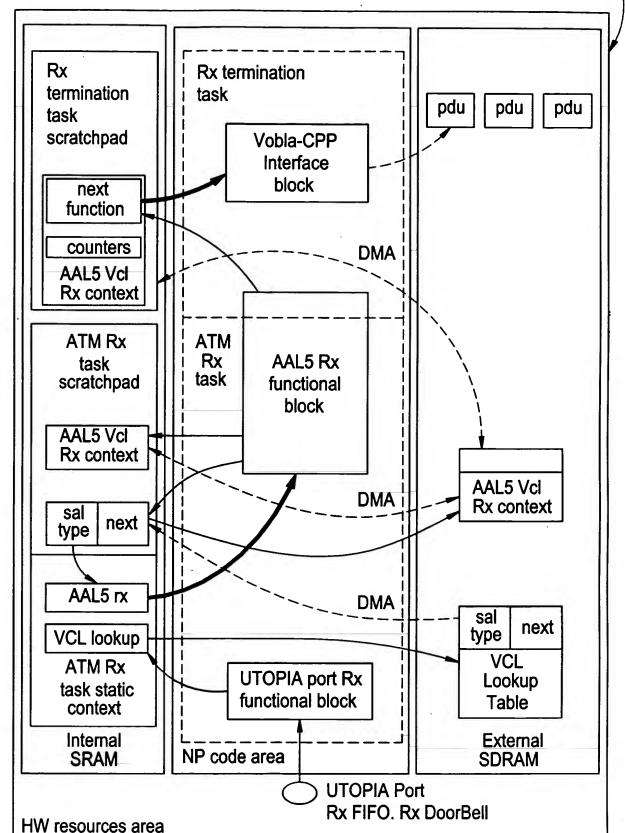




TOOMFJUL TOOMS

FIG. 84

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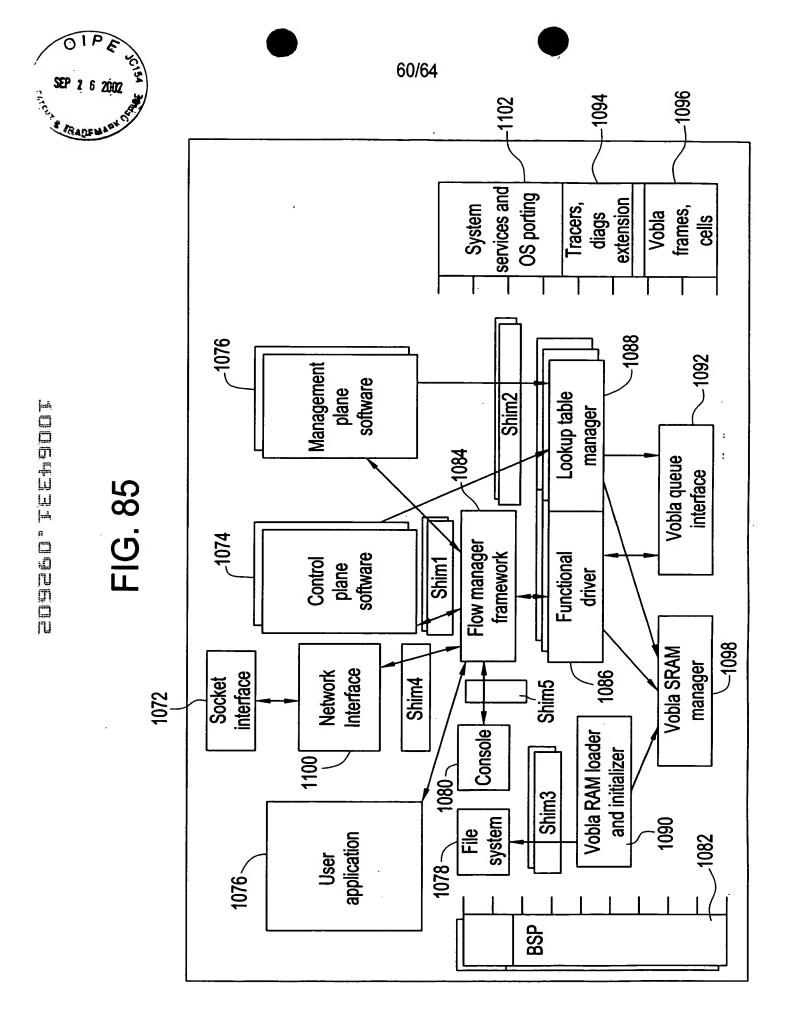


FIG. 86

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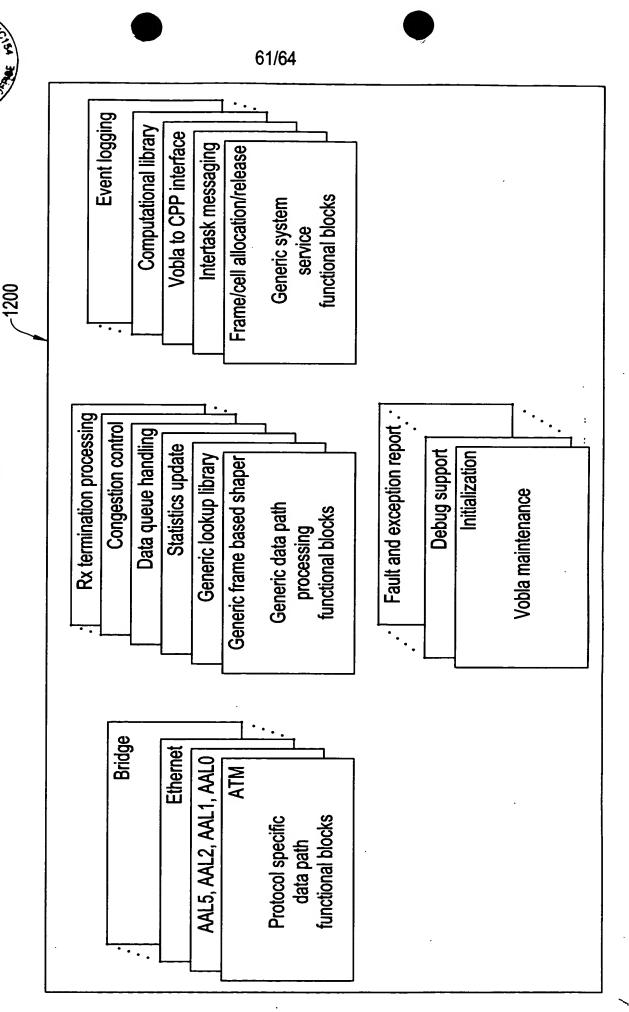




FIG. 87 PRIOR ART

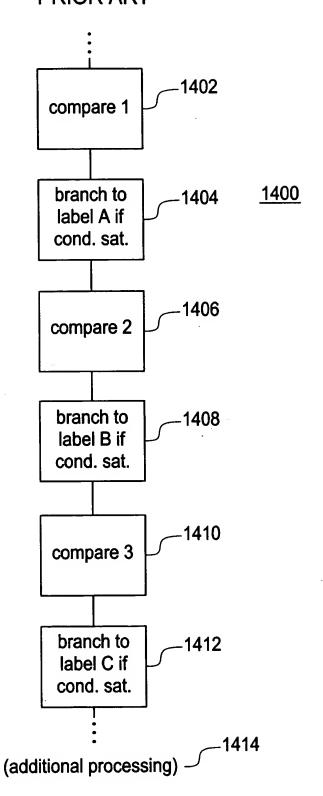




FIG. 88

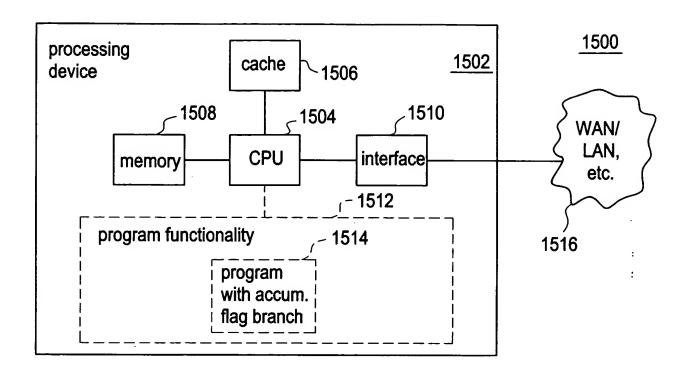


FIG. 89

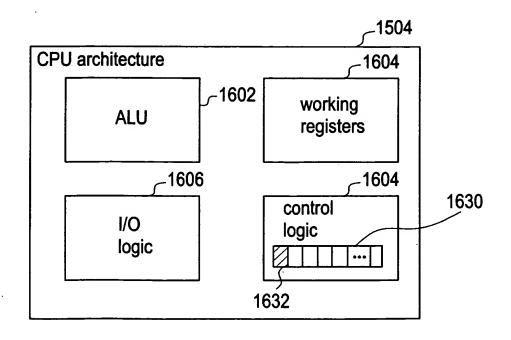


FIG. 90

